METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS

[Description] **FIELD OF THE INVENTION**

The present invention relates to a method for testing digital
protective circuits in which data processing means are used to
simulate the current and voltage response of a power supply

5   network by outputting digital current and voltage signals in
cycles; corresponding currents and voltages are generated from
the digital current and voltage signals and supplied to a
protective circuit to be tested; and tripping signals from the
respective protective circuit are detected.

BACKGROUND INFORMATION

10 A method of this type is [generally known from] **described in**
"Elektrizitätswirtschaft", Vol. 78 (1979), No. 1, pages 18 to
23. [According to a] **In this** method [of this type], a data
processing system emits digital current and voltage signals in

15 cycles on the basis of the current and voltage ratios present
in a power supply network; the data processing system thus
forms a network model. Corresponding currents and voltages can
be generated from the digital current and voltage signals and

20 supplied to a protective circuit to be tested. When currents
and voltages corresponding to an error in the simulated power
supply network are applied to the protective circuit to be
tested, the latter generates a tripping signal. The occurrence
of the tripping signal can be assigned to the respective

25 currents and voltages to draw conclusions about the tripping
performance of the respective protective circuit to be tested.

To test the digital protective circuits under conditions that
are as close to reality as possible, it is useful to control

30 the data processing system simulating the power supply network
and representing a network model when detecting a tripping
signal so that the data processing system also outputs network
error-specific digital current and voltage signals. Because

this requires longer computing times than are needed for digital current and voltage signals that indicate a normal, continuous variation of currents and voltages, it is [conceivable] **possible** to use a very high-speed data

5   processing system and to have the latter output network error-specific digital current and voltage signals when a tripping signal is emitted by the respective protective circuit to be tested. However, a data processing system of this type is highly complex and therefore very expensive to

10   produce or purchase.

SUMMARY

An [The] object of the present invention is to provide a method for testing digital protective circuits in which a

15   conventional data processing system, such as a personal computer, can be used to test digital protective circuits under close-to-real conditions even using network error-specific digital current and voltage signals from a data processing system of this type.

20

This object is achieved with a method according to the present invention [of the type mentioned in the preamble] in that when the test of a protective circuit begins, the output digital current and voltage signals are first buffered consecutively,

25   and, upon reaching a specific quantity of buffered digital current and voltage signals, the oldest buffered digital current and voltage signals in each case are output in cycles and supplied to the respective protective circuit to be tested, and more recent output digital current and voltage

30   signals are rebuffered; upon the occurrence of a tripping signal, **a** data processing [means output] **arrangement outputs** network error-specific digital current and voltage signals, while the oldest buffered digital current and voltage signals in each case continue to be output in cycles, and the network

35   error-specific digital current and voltage signals are each rebuffered after being output.

German Patent No. 150 947 describes computer-supported testing of protective circuits in which non-stationary processes that are simulated with digital models, for example, are stored and the stored data is provided to the test object in a specific

5   order. All of the data is accepted before sensing the protective circuit. To test a test object, the data is sent to the test object in a specific order and the signal response of the test object is detected.

10   **One** [A significant] advantage of the method according to the present invention is that it can be carried out with a comparatively simple data processing system design in the form of a conventional personal computer. This is due to the fact that, in the method according to the present application, the

15   digital current and voltage signals output by the data processing system are first buffered consecutively until a specific quantity of buffered digital current and voltage signals is reached. The buffered signals are output in cycles during the test procedure. This applies even if a tripping

20   signal is generated. Nevertheless, the occurrence of the tripping signal causes the data processing system to output network error-specific digital current and voltage signals, which results in a longer computing time than would be needed with an undisturbed, simulated network state, due to the

25   complicated arithmetic operations required. The network error-specific digital current and voltage signals are also buffered. The quantity of digital current and voltage signals is thus replenished. The problem of [essentially] insufficient computing speed of the relatively simple data processing

30   system used is thus overcome to a certain extent by buffering the signals.

The present invention takes advantage of the fact that, in situations where a protective circuit is used, the tripping

35   signal generated by the circuit when an error occurs in the network to be monitored is immediately applied to a switch,

MARKED-UP VERSION OF

SUBSTITUTE SPECIFICATION

usually a circuit-breaker; however, the circuit-breaker to
which this signal is applied does not immediately open its
contacts, but instead requires a certain switch response time
for this purpose, which ranges between approximately 20 and

5   100 ms—and is frequently around 60 ms. Only at the end of the
switch response time do new current and voltage ratios
actually occur in the network, a fact that must also be taken
into account when testing a digital protective circuit with
the method according to the present invention.

10

In light of this fact, it is deemed advantageous in the method
according to the present invention to determine the specific
quantity of digital current and voltage signals buffered in
cycles on the basis of the response time of switches for which

15   the protective circuits to be tested are to be used, taking
the cycle time into account. With the method according to the
present invention, this ensures that the network
error-specific digital current and voltage signals that
correspond to the changed network conditions are output at the

20   end of the switch response time, just like in a real
situation.

In the method according to the present invention, the buffered
digital current and voltage signals can be output at [a

25   variable output rate. It is viewed as advantageous to output
the buffered] **an interval that corresponds to the duration of**
a tripping signal-free test period needed to output further
digital current and voltage signals [at an output rate that
corresponds to the duration of a tripping signal-free test

30   period needed to output further digital current and voltage
signals] in each case[, thus achieving cyclical output. While
the quantity of buffered current and voltage signals in a
method of this type is used up after a certain amount of time
following a simulated network error, it frequently is fully

35   sufficient for a practical simulation. The special advantage
is that, in this embodiment of the method according to the

present invention, the output frequency of the digital current and voltage signals can be more or less doubled compared to the method described in the preamble].

5   In another embodiment of the method according to the present invention, the buffered digital current and voltage signals are output at an output rate that is greater than the duration of a tripping signal-free test period needed to output digital current and voltage signals[. In this embodiment of the method

10   according to the present invention, the quantity of buffered digital current and voltage signals is replenished after a tripping signal occurs so that, according to this method embodiment, simulations of practically any duration can be carried out.

15   The present invention also concerns a test arrangement including a data processing system that simulates the current and voltage response of a power supply network in the form of a network model by outputting digital current and voltage

20   signals in cycles, and including a converter unit, located downstream from the data processing system, which generates corresponding currents and voltages from the digital current and voltage signals and supplies them to a protective circuit to be tested.] **in each case.**

25

An arrangement of this type is also [generally known from] **described in** the publication cited above. To further develop an arrangement of this type so that it can also take into account network error-specific digital current and voltage

30   signals following the generation of a tripping signal, without requiring a great deal of computing power, the data processing system is assigned, according to the present invention, a buffer in which the output digital current and voltage signals are first buffered consecutively; a sensing arrangement that

35   detects tripping signals from the respective protective

circuit is connected on the output side to the data processing
system.

The arrangement according to the present invention differs
from the arrangement described in German Patent No. 150 947 in
that it has a storage device in the form of a buffer in which
data is entered during the test and from which data is output
during the test. A further difference lies in the provision
of a sensing arrangement that controls the data processing
system upon the occurrence of a tripping signal from the
respective protective circuit to be tested so that the data
processing system sends network error-specific data to the
buffer.

One significant advantage of the arrangement according to the
present invention is that it can make do with a data
processing system in the form of a conventional personal
·computer and can therefore be produced at comparatively little
cost; the additional cost of the buffer is comparatively low.
A further advantage is that the test can also be carried out
with network error-specific current and voltage signals after
a tripping signal occurs, using a simple circuitry design.

In the arrangement according to the present invention, the
buffer advantageously has a sufficiently large storage
capacity to buffer all current and voltage signals output
during a tripping signal-free test period corresponding to the
response time of switches provided for interaction with the
protective circuits to be tested.

The buffer is advantageously a ring buffer, i.e. a buffer in
which new data is stored for current and voltage signals
previously output by the data processing system.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. [To further explain the present invention, Figure] 1
shows a block diagram [illustrating] **of** one **example** embodiment
of the method according to the present invention[, while
Figure]_._

5 **Fig.** 2 shows three diagrams illustrating the operation of the
buffer shown in the block diagram.

DETAILED DESCRIPTION

Figure 1 shows a block representing a data processing system
10 1, which is formed by a conventional personal computer. Data
processing system 1 includes a network model 2 that can be
provided by a NETOMAC simulation program, which is described
in detail in the publication mentioned [in the preamble].
above. Network model 2 outputs digital current and voltage
15 signals J' and U', respectively, via a bus 3, based on the
performance of a power supply network to be simulated. These
digital current and voltage values [I'] **J'** and U',
respectively, are further processed in an interface module 4,
which is also used for internal system communication.
20 Interface module 4 is provided with a buffer in the form of a
ring buffer 5 in which a specific number of output digital
current and voltage signals J' and U', respectively, are
buffered. When the test of a digital protective circuit 6
begins, digital current and voltage signals J' and U',
25 respectively, emitted by network model 2 are first buffered in
ring buffer 5 in cycles, i.e. based on the system clock. The
storage capacity of this ring buffer 5 is selected in view of
the system clock cycle so that the buffer becomes full at the
end of a period that corresponds to response time Tls of
30 switches (not illustrated) for which protective circuit 6 to
be tested is to be used.

When a time Tls of this type elapses after the beginning of
the test, a buffered value of current and voltage signal Jz
35 and Uz, respectively, is output from ring buffer 5 with the
next system clock cycle and transmitted via a bus 7 to a

further interface module 8, which applies a load to a digital-analog converter 10 via an additional bus 9. In this digital-analog converter 10, currents J and voltages U, respectively, corresponding to the respectively transmitted

5   digital current and voltage values are generated and supplied to protective circuit 6 to be tested via amplifiers 11 and 12. Diagram A of Figure 2 shows the variation over time t of voltage U generated in this manner. Likewise, Diagram B shows generated current J over time, which initially appears to have

10   a value of zero only due to the scale selected. Diagram C of Figure 2 shows number n of the digital current and voltage values stored in ring buffer 5 over time t. [We can see that, prior] **Prior** to a time T1 after the beginning of the test, only ring buffer 5 is first filled with digital current and

15   voltage values at time zero. After time T1 is reached, the amount of data entered into the ring buffer cyclically equals the amount of data output. This means that number n of stored data remains the same after time T1.

20   In the illustrated example, it is assumed that protective circuit 6 to be tested emits a tripping signal S at time T2 as a result of current and voltage values J and U that it receives. This tripping signal S is detected by a sensing arrangement 13 and passed on to the one interface module 4 via

25   a further interface module 8 over a bus 14. The one interface module 4 subsequently causes network model 2 to output, via a bus 15, digital current and voltage signals that are network error-specific, i.e. would occur in the event of a short-circuit in the simulated network. As shown in Diagrams A

30   and B of Figure 2, fluctuations occur over a period ΔT, the calculation of which in network model 2 requires a relatively large amount of computing power and thus takes a relatively long time so that these network error-specific digital current and voltage signals are output at a relatively slow rate.

35   Because the buffered digital current and voltage values continue to be output from ring buffer 5 in cycles, although

not at the same rate at which network error-specific digital
current and voltage values are generated by network model 2,
the quantity of buffered data in ring buffer 5 starts to
decrease from time T2 onward, as clearly illustrated by
5   Diagram C of Figure 2.

If [we assume] **it is assumed** that [output rate Δt of] digital
current and voltage signals J' and U' in the network model **are**
output at an interval Δt that is equal to required computing
10   time tmin when a tripping signal S is not present and a
fluctuation does not occur, ring buffer 5 cannot be completely
refilled. However, if [we assume] **it is assumed** that the
computing time of network model 2 is tmax after a tripping
signal occurs, fluctuations can occur in response time Tls of
15   the switches during a simulation Tls/(tmax-tmin) until the
buffer is empty. Assuming typical values for tmax=1 ms,
tmin=0.5 ms, and Tls=60 ms, 120 fluctuations can occur during
the simulation until ring buffer 5 can no longer provide any
more output data. In practice, this is entirely sufficient.

20   In the illustrated example, it is assumed that [output rate]
interval Δt is greater than required computing time tmin of
network model 2 before a tripping signal S occurs, and that
Δt>tmin. Filling time tf of ring buffer 5 can then be
25   determined with the following equation:

$$tf = \left(\frac{t\max - F \cdot t\min}{F - 1} \right) \cdot F$$

where F=Δt/tmin. The assumptions described above by way of an
30   example then yield a filling time tf of roughly 5 ms. This
means that simulations lasting 5 ms without any fluctuations
are sufficient to compensate for the time lost by the
fluctuation calculation and to completely refill ring buffer

5. This gives the system a 90% increase in performance in this case. As clearly shown by Figure C, simulations of practically unlimited length can be carried out in this case because the switch never carries out a sufficiently large number of switching operations in a short period of time to allow buffer 5 to be emptied.

Abstract

A method and an arrangement for testing digital protective
circuits in which data processing means are used to simulate a
5   power supply network by outputting digital current and voltage
signals in cycles. Corresponding current and voltages are
generated from these signals and supplied to a protective
circuit to be tested. [

]To test protective circuits under conditions that are as
10   close to reality as possible with a method of this type, using
a comparatively simple data processing system design, the
output digital current and voltage signals [(J′, U′)] are
first buffered consecutively when the test of a protective
circuit [(6)] begins. Upon reaching a specific quantity of
15   buffered signals[(Iz, Uz)], the oldest buffered signals [(Iz,
Uz)] in each case are output in cycles, and more recent output
signals [(J′, U′)] are buffered. Upon the occurrence of a
tripping signal, output continues in cycles, and data
processing means output and buffer network-specific digital
20   current and voltage signals.
[
FIG 1]